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Patentanmeldung Nr. Patent application No. Demande de brevet n°

03103757.5

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

R C van Dijk

Anmeldung Nr:
Application no.: 03103757.5
Demande no:

Anmeldetag:
Date of filing: 10.10.03
Date de dépôt:

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Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
Si aucun titre n'est indiqué se referer à la description.)

Electronic device and carrier substrate

In Anspruch genommene Priorität(en) / Priority(ies) claimed /Priorité(s) revendiquée(s)
Staat/Tag/Aktenzeichen/State/Date/File no./Pays/Date/Numéro de dépôt:

Internationale Patentklassifikation/International Patent Classification/
Classification internationale des brevets:

H01L23/498

Am Anmeldetag benannte Vertragstaaten/Contracting states designated at date of filing/Etats contractants désignées lors du dépôt:

AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL
PT RO SE SI SK TR LI

Electronic device and carrier substrate

The invention relates to an electronic device comprising

- a semiconductor device provided with a plurality of bond pads, of which bond pads a first portion is defined for ground connection and a second portion is defined for voltage supply and a third portion is defined for signal transmission, and
- a carrier substrate comprising a layer of dielectric material and having a first side and an opposed second side, with at each side an electrically conductive layer, at which first side bond pads are present corresponding to the bond pads of the semiconductor device, and at which second side contact pads for external coupling are provided, the contact pads and the bond pads being electrically interconnected according to a desired pattern, the contacts pad being subdivided in a first, a second and a third portion corresponding to the portions of the semiconductor device, the first and second portions of the bond pads are present laterally in an inner area and the third portion is present in an outer area laterally around the inner area.

The invention also relates to such a carrier substrate.

Such an electronic device and such a carrier substrate are known from US-A 6,448,639. The known device is known as a ball grid array package. This type of package is well known for a variety of integrated circuits, with as main advantages its easy placement on an external carrier with solder balls, and the ability to provide a very large number of contact pads, and thus very many signal connections, generally known as I/O paths.

The known carrier substrate is provided with two electrically conducting layers, which has the advantage of reducing the cost price of such a package. The first and second portions of the contact pads for ground and voltage supply connection are disposed right under the corresponding bond pads at the first side of the carrier substrate. These bond pads are embodied as concentric ground and power rings, which are coupled with bond wires to the bond pads of the semiconductor device. Due to this construction the connections

between the bond pads and the corresponding contact pads are short, which leads to an improved electrical and thermal performance.

It is a drawback of the known device that the ground bounce voltage is still rather high. This ground bounce voltage is defined as the dynamic voltage difference between a ground plane in an external carrier to which the electronic device is attached and the ground connection in the semiconductor device. The higher the ground bounce voltage, the smaller the difference between voltage supply and ground voltage in the semiconductor device, and thus the smaller the margin of operation. This smaller margin of operation will increase the sensitivity for external disturbances and gets more critical with advances in semiconductor technology. The smaller the channel length, the smaller the margin of operation is anyway. Alternatively the ground bounce voltage could be nivellated by a higher voltage supply, but this leads to a higher the required thermal dissipation. Moreover, therewith the problem is not resolved, as the problem with the ground bounce voltage is that it is unpredictable.
In other words, it is a first object of the invention to provide an electronic device of the kind mentioned in the opening paragraph with a reduced ground bounce voltage.

It is a second object of the invention to provide a carrier substrate that is suitable for use in the device of the invention.

The first object is achieved in that the semiconductor device is coupled to the carrier substrate in a flip-chip orientation. The bond pads and the contact pads for voltage supply and ground connection are located correspondingly, so as to provide a direct path from the contact pads at the substrate to the corresponding bond pads of the semiconductor device. Furthermore, the pads of the first and second portions are arranged such that at least one direct path dedicated to voltage supply connection acts as a coaxial center conductor.

The device of the invention has the merit that voltage supply connections are present as coaxial structures. Therewith, the effective inductance for each of these power paths is reduced by the mutual inductance between the power – or voltage supply - and the ground. This results in the desired lower ground bounce voltage. The effect of the coaxial structure is substantial; the effective inductance of the ground path can be lower by more than 50%.

It is an advantage of the present structure, that the bond pads of the voltage supply connection at the first side of the carrier substrate can be made in the conductive layer present there. In other words, no additional redistribution layer is needed, and a substrate

with conductive layers at the opposite sides only can be used. This results in cost reduction in comparison with a carrier substrate with internal conductors.

In an advantageous embodiment, the bond pads of the first and second portion form a joint array, having an edge and an inner area, and the bond pads of the second portion at the edge are provided with ESD protection structures, the bond pads of the second portion in the inner area being free of such ESD protection structures. As the conductivity of the power path is good enough, the voltage gradient shall be minimal during an ESD stress. Hence, the number of ESD protection structures can be limited.

In a further modification, the pads for ground and supply connection are arranged according to a chessboard pattern. This has first of all the advantage that the resulting structure is miniaturized. The contact pads can thus be of a size suitable for assembly to a printed circuit board, while at the same time the dimensions of the semiconductor device need not to be increased.

Particularly for this modification, the bond pads at the semiconductor device will be divided in a regular pattern which covers the complete surface area. They are thus also provided on top of the active area. The mechanical support of the bond pads may therefore be strengthened, for instance in that the bond pads are present on top of the passivation layer. However, this is not considered necessary in any case. In any case, there is no need for staggered pads at the edge of the semiconductor device. Furthermore, a single ring of bond pads for signal transmission (I/O pads) may be used, which reduces the complexity at once.

It is a first advantage of the chessboard pattern that sufficient pads can be assigned for the voltage supply of the semiconductor device, and particularly the core functionality thereof. An array of 10 by 10 pads provides sufficient power for the use of DC currents of more than 4 Ampère in integrated circuits with channel length of 0.12 μm.
It is a second advantage of the chessboard pattern that the IR drop can be minimized, and will be determined by the semiconductor device. The upper metals of the interconnect structure in an integrated circuit have a smaller thickness than those at the carrier substrate. Hence, the losses at the substrate are lower. It turns out that this holds if the voltage supply and ground connections are distributed equally over the inner area of the carrier substrate, hence that there is a chessboard pattern with equal conditivity in the two orthogonally directed, lateral directions.

The IR drop is particularly relevant for advanced IC processes. An IR drop of 10% was allowed for old CMOS processes, whereas it is only 5% for advanced IC processes

with a channel length of 0.18 μm or less. However, the average supply current increases on decreasing the supply voltage for those advanced IC processes. By parallel switching of the package interconnect, at least for the core, the IR drop on the IC is diminished.

In a further embodiment the layer of dielectric material extends from the first to the second side in the substrate. In other words, use is made of a dielectric substrate. This leads to cost reduction. The material of the substrate can thus be a suitable material such as polyimide, polymer strengthened glass fibers, FR-4 (an epoxy resin), FR-5 and BT-resin. Alternative materials include such materials filled with particles with a relatively high dielectric constant (such as perowskite type materials), ceramic materials including SiO_2, Al-C-O-N, materials obtainable by sintering a matrix of thermally conductive material with embedded semiconductor particles. Particularly the combination of a matrix materials and embedded particles is preferred, as this allows optimalisation of a range of parameters, including the dielectric constant, the coefficient of thermal expansion, the mechanical strength and the thermal conductivity. Examples are given in WO01/15182, EP-A 743929, EP03075079.8 (PHNL030040, not prepublished). The choice of the material is rather wide, in that no internal conductors are needed.

In a further embodiment, the bond pads of the third portion and the corresponding contact pads for external coupling are mutually interconnected through interconnects defined in the conductive layer at the first side of the carrier substrate, and through vertical interconnects through the carrier substrate which on perpendicular projection on the conductive layer at the second side have a substantial overlap with the contact pads for signal transmission. This embodiment is particularly suitable to reduce the complexity of the carrier substrate. Additionally, it allows some further modifications that are beneficial:

In a first modification use is made of different supply voltages for different parts of the semiconductor device. Particularly, the semiconductor device can be divided into the core functionality and the peripheral functionality. The inner area of the substrate is then used for the voltage supply and ground connection to the core. The outer area is used for the signal transmission, the voltage supply and the ground connection to the periphery. The division of a semiconductor device, and particularly an integrated circuit, into core and periphery is suitable for all ICs to limit thermal dissipation and for mixed-signal ICs especially.

In a further modification hereof, the contact pads in the peripheral area are defined in subgroups, each subgroup comprising one contact pad for voltage connection or one contact pad for ground connection, and several contact pads for signal transmission, all

of the pads for signal transmission having the contact pad for either voltage or ground connection as a neighbouring pad. Particularly, the contact pad for voltage or ground connection will be the center ground pad of the group. This subdivision in subgroups allows that there is a minimum distance between a signal path in one direction and a signal path in the reverse direction (the contact pad for either ground or voltage supply). Such a subdivision is particularly important to enforce a proper transmission path from the carrier substrate to an external carrier. Its implementation is thus needed at the level of the solder balls for placement of the device on an external carrier, and hence in the contact pads at the second side of the carrier substrate.

In a second modification, a ground plane is defined in the conductive layer at the second side of the carrier substrate, and the mutual distance between the interconnects and the dielectric thickness of the carrier substrate are chosen such that the interconnects have transmission line characteristics. Any impedance losses at the signal transmission are herewith substantially limited.

In a third modification, both modifications are applied and additionally the periphery is provided with an additional on-chip decoupling capacitor. In this manner the communication between the core functionality and the peripheral functionality is optimized.

In another modification a mechanical stiffner layer is present at the first side of the carrier substrate. This solution allows a further reduction of the thickness of the dielectric layer, while not distorting the transmission line character of the interconnects. The transmission line character of the interconnects leads to a reduction of the thickness of the carrier substrate to 100 or 50 μm or potentially even less to obtain the desired transmission line characteristics. In order that the device nevertheless has the desired mechanical stability an encapsulation could be applied. This is, however, not preferred for reasons of thermal management. The use of a dielectric stiffner, which leaves the bond pads at the first side exposed, is a practical solution. It is preferred but not necessary that the dielectric stiffner is made from the same material as the dielectric material of the carrier substrate. Dependent on the stiffner material used an additional spacer may be needed to maintain the transmission line characteristics.

In to a further embodiment a spacer layer is present at the first side of the carrier substrate, which spacer layer is covered by a heat dissipation layer, which heat dissipation layer is in thermal contact with the semiconductor device at a face thereof opposite to the face comprising the bond pads. This is an option to improve the thermal

management of the device of the invention. It may well be that the spacer is formed by the mechanical stiffner layer.

In a modification hereof, the heat dissipation layer is connected thermally to a heat sink at the carrier substrate. The presence of a heat dissipation layer is not sufficient in itself to improve the thermal management, as it has turned out that the passive cooling at the interface of such heat dissipation layer and air is not gigantic. To improve it, active cooling could be used, such as heat pipes, which however have the disadvantage of being large. Preferred is then the provision of a heat connection to a heat sink at the carrier substrate. The heat connection may include a component that is assembled to the carrier substrate as the semiconductor device is. Alternatively, use can be made of thin and thick film techniques, for instance in that a throughhole is provided in the spacer. The heat sink of the substrate may be embodied as the ground plane at the second side of the substrate.

In an even further embodiment the device is further provided with a supply series inductor. Such a series inductor preferably has a magnitude in the range of 0,5-1,0 μH. It is a nice implementation to sustain operation over a clock period. Preferably, the inductor is provided as a discrete component at the external carrier, and more preferably within an area corresponding to the core area. Alternatively, the inductor can be integrated in either the external carrier or the carrier substrate. Preferably, the dielectric material is then suitable provided with magnetic particles, for instance of a ferrite material, such as to enhance this inductance.

It is observed that the electronic device of the invention comprises at least one semiconductor device. Generally, this semiconductor device is an integrated circuit. Alternatively, more than one semiconductor device may be provided, such as an integrated circuit and diodes; an amplifier and a transceiver; an amplifier and other RF components such as filters and antenna switches; or a first and a second integrated circuit. In the case of two integrated circuits, the core functionality may be present in the first integrated circuit, and the peripheral functionality may be present in the second integrated circuit.

In a further embodiment of the invention, a second electric device is present, which electric device is provided with a direct path for ground and voltage supply connection from its bond pads to the second side of the carrier substrate, at which second side contact pads for ground and voltage supply connection are present. The construction of direct provision of voltage supply and ground to a semiconductor device can be repeated for a second device. The mutual interconnection of the devices can be realized by interconnects at the first side of the carrier substrate. If present, the signal transmission connections may be

integrated into one array. These arrays are usually ring shaped according to the JEDEC-standards of ball grid arrays. The second electric device is preferably a semiconductor device, but may alternatively be a sensor, such as a magnetoresistive sensor, a resonator, such as a bulk acoustic wave resonator, a microelectromechanical system (MEMS) element, etcetera.

These and other aspects of the device and the carrier substrate of the invention will be further explained with reference to the Figures, in which:

Fig. 1 shows a diagram of the device of the present invention;

Fig. 2 shows diagramatically a cross-sectional view of the device;

Fig. 3 shows diagramatically a bottom view of the device; and

Fig. 4 shows diagramatically a top view of the device.

The Figures are not drawn to scale and equal reference numerals refer to similar or equal parts. The Figures show one preferred embodiment, but many modifications hereof will be apparent to the skilled person.

Fig. 1 is a graph in which the device 100 of the present invention is depicted. The device 100 comprises a semiconductor device 10, which is in this case an integrated circuit. The semiconductor 10 comprises a core functionality 110 and a peripheral functionality 210. The device 100 further comprises a carrier substrate 20, that is provided with a core area 31 and a peripheral area 32. The core functionality 110 comprises the active elements 112 as well as a decoupling capacitor 111, and is provided with voltage supply connections 42 and ground connections 41. By means of the supply decoupling topology with the core decoupling, the contribution to ground bounce, i.e. RF emission from the core can be reduced effectively.

The peripheral functionality 210 comprises I/O means 212 and means for tuning 211, in this case a decoupling capacitor placed in series with the I/O means 212. The peripheral functionality 210 is further provided with connections 43, for voltage supply, ground and signal transmission. The ground connections 41, 43 of the peripheral and the core functionality 110,210 are mutually interconnected through an interconnect 22 in the carrier substrate 20. The decoupling capacitor 211 is herein used to stabilize the behaviour. The carrier substrate 20 further comprises contact pads 61, 62, 63, 64, 65 for connections to a printed circuit board.

Fig. 2 shows a cross-sectional view of an embodiment of the device 100 of the invention. Fig. 3 shows the device 100 of this embodiment from the second side of the carrier substrate 20, at which the contact pads 61-65 for external connection are present. Fig. 4 shows the device from the first side of the carrier substrate 20. The layout of the integrated circuit 10 is shown as if it were transparent, and shows the side 18 with bond pads 11-13. It is observed that in Fig. 3 and 4 only part of the substrate are shown; the substrate usually extends laterally, and the contact pads 63-65 generally forms a closed ring around the integrated circuit. Therewith the embodiment is an example of a typical ball grid array package, as the skilled person will understand. Such a package is preferred, but the invention is not limited thereto. It is furthermore observed that Fig. 2 is not a true cross section, as the skilled person will find out on comparison with Fig. 3.

The device 100 of this embodiment comprises a carrier substrate 20 is subdivided into a core area 31 and a peripheral area 32. The carrier substrate 20 has a first side 21 and a second side 22. It comprises a body 20A of dielectric material and electrically conducting layers 20B, 20C at the first and second side 21,22 respectively. The dielectric material is in this case an epoxy resin (FR-4) with a thickness of about 80 μm, and the electrically conducting materials are of copper. The resolution of interconnects and other tracks defined in the copper is in the order of 50 μm and with a minimal distance between neighbouring tracks of 100 μm, in this embodiment.

The carrier substrate 20 is provided herein with a ground plane 51 at the second side 22 of the substrate, extending in the peripheral area 32, and with interconnects 53, that have a transmission line character. The bond pads 43 for the peripheral functionality are provided near to the edge of the core area 31, such that the transmission lines are well defined and their behaviour not negatively affected by bond wires or the like. At the first side 21 a mechanical stiffening layer 29 is present, which provides additional mechanical stability. The stiffening layer 29 has in this case a thickness of about 300 μm and is provided in the same material as the body 20A.

The integrated circuit 10 has a first side 18 at which it is provided with bond pads 11,12,13 (see figure 3). The bond pads 11 are those of the first portion for ground connection. The bond pads 12 are those of the second portion for voltage supply connection. The bond pads 13 include those of the third portion for signal transmission. In this embodiment, in which the integrated circuit is provided with core functionality 110 and peripheral functionality 210, the bond pads 13 are also used for the provision of voltage supply and ground connections of the peripheral functionality 210. The bond pads 11,12 are

distributed evenly over the available surface area of the integrated circuit 10, and according to a chessboard pattern. On assembly on the carrier substrate 20, the result is a direct path from the bond pads 11,12 to the corresponding contact pads and solder balls at the second side of the carrier substrate 20.

The integrated circuit in the invention is provided with core functionality and with peripheral functionality. In the invention, separate areas are defined in the carrier substrate 20 for each of the functionalities: a core area 31 for the core functionality and a peripheral area 32 for the peripheral functionality. In the embodiment the peripheral area 32 is positioned laterally around the core area 31. This is preferred, but not necessary. Specific bond pads are present at the first side 21 of the carrier substrate 20 for the core functionality (42) and the peripheral functionality (43). The bond pads for the peripheral functionality 43 include the bond pads for signal transmission and voltage supply. The bond pads for the core functionality 42 include the bond pads for the voltage supply. In addition, there are bond pads for ground connections (41).

The core area 31 and the peripheral area 32 of the carrier substrate 20 are designed differently. In the core area 31, the bond pads 41,42 at the first side 21 are directly connected to the second side 22, so as to minimize inductive losses. The contact pads 61 for ground connection are positioned directly below the corresponding bond pads 41. In order to have a ground that is as standardized as possible, the bond pads 41 for ground are mutually interconnected through a ground plane 52 at the first side 21 of the carrier substrate 20. The contact pads 62 for voltage supply connection are coupled to the corresponding bond pads 42 through interconnects 67 at the second side 22 of the carrier substrate 20 to the vertical interconnects 66.

The peripheral area 32 of the carrier substrate 20 is provided with a ground plane 51 at its second side 22. At the first side 21 interconnects 53 are defined, so as to connect the bond pads 43 with corresponding contact pads 63, 65. Due to the presence of the ground plane 51 at the second side 22, and a mutual distance between neighbouring interconnects 53 that is preferably larger than the thickness of the body 20A, the interconnects 53 behave as transmission lines. There inductive losses are therewith reduced for at least 90%, and generally even about 95%.

The interconnects 53 end up at vertical interconnects 73, 75, as shown in Fig. 4. The interconnects 75 are corresponding to the contact pads 65 for voltage supply connections of the peripheral functionality. The interconnects 73 are corresponding to the contact pads 63 used for signal transmission. Additionally, there are also contact pads 64 for

ground connections of the peripheral area 32. These contact pads 64 are interconnected to their bond pads 41 through the ground plane 51 at the second side 22 of the carrier substrate 20. The contact pads 64 for ground are positioned at the outer periphery of the contact pads array, generally a ball grid array. This provides some protection against electromagnetic inference.

Some of the contact pads 65 meant for voltage supply connections could be used for ground connections. This is a matter of design and depends on the required number of voltage supply connections and ground connections to an external carrier. It is however preferred that the contact pads 63-65 are subdivided in subgroups 164, 165. In the subgroups 164,165 up to eight contact pads 63 for signal transmission are present around a center contact pad 64, 65 that is either a pad for ground or for voltage supply. In this manner a signal path and its signal return can be neighbouring, and hence the distance between both is minimal. This enforces a proper transmission path for the carrier substrate 20 to an external carrier.

This embodiment with the flip-chip orientation of the semiconductor device 10 to the carrier substrate 20 has substantial advantages. First of all, there is no need for an additional bond pad layer at the first side 21 of the carrier substrate 20, which is needed for the wirebonding. There is no need for a redistribution layer (i.e. through the interconnects 66, 67) or a staggered pad array either. The solder balls between the bond pads 11,12, 13 of the integrated circuit and the bond pads 41, 42, 43 at the carrier substrate 20 can be provided directly on the electrically conductive layer 20B.

Secondly, both the contact pads 61,62, as well as the corresponding bond pads 41,42 and 11,12 are arranged in a 'chessboard'-pattern. In such a pattern each closest neighbour of a pad for voltage supply 12,42,62 is a pad for ground 11,41,61 and vice versa. Herewith the ball grid array has a coaxial structure, with a reduction of the effective inductance with about 50%, and a lower groundbounce voltage. The bond pads 11,12 at the integrated circuit 10 are herein provided in an inner area. These pads 11,12 are – seen in perpendicular projection on the substrate of the integrated circuit – overlapping with the active region. Such a design of bond pads is also known as bond pads on active. They may be provided on top of a passivation layer, in order to provide sufficient strength.

Thirdly, due to the good conductivity (low impedance, low losses) of the interconnect of the core voltage supply in the carrier substrate, the number of ESD protection structures can be reduced. In fact, they are needed only at the outer edge of the core area 31. This is based on the insight that the voltage gradient in the core area 31 shall be minimal

during an ESD stress, as a consequence of the good conductivity. For the ground connections, ESD protection structures are needed in the core area 31 and in the peripheral area 32.

Fourthly, the thermal management of the device 100 can be improved in that a heat spreading layer 15 is provided at the first side 21 of the carrier substrate and the backside of the integrated circuit 10, e.g. the side of the facing away from the bond pads 11-13. It is particularly preferred that the semiconductor substrate of the integrated circuit 10 is thinned, therewith reducing the path of thermal resistance to the heat spreading layer 15.

CLAIMS:

1. An electronic device comprising

- a semiconductor device provided with a plurality of bond pads, of which bond pads a first portion is defined for ground connection and a second portion is defined for voltage supply and a third portion is defined for signal transmission, and
- a carrier substrate comprising a layer of dielectric material and having a first side and an opposed second side, with at each side an electrically conductive layer, at which first side bond pads are present corresponding to the bond pads of the semiconductor device, and at which second side contact pads for external coupling are provided, the contact pads and the bond pads being electrically interconnected according to a desired pattern, the contacts pad being subdivided in a first, a second and a third portion corresponding to the portions of the semiconductor device, the first and second portions of the bond pads are present laterally in an inner area and the third portion is present in an outer area laterally around the inner area,

wherein

- the semiconductor device is coupled to the carrier substrate in a flip-chip orientation, and
- the bond pads and the contact pads for voltage supply and ground connection are located correspondingly, so as to provide a direct path from the contact pads at the substrate to the corresponding bond pads of the semiconductor device, and
- the pads of the first and second portions are arranged such that at least one direct path dedicated to voltage supply connection acts as a coaxial center conductor.

2. An electronic device as claimed in Claim 1, wherein the bond pads of the first and second portion form a joint array, having an edge and an inner area, and the bond pads of the second portion at the edge are provided with ESD protection structures, the bond pads of the second portion in the inner area being free of such ESD protection structures.

3. An electronic device as claimed in Claim 2, wherein the pads for ground and supply connection are arranged according to a chessboard pattern.

4. An electronic device as claimed in Claim 1, wherein layer of dielectric material extends from the first to the second side in the substrate.

5. An electronic device as claimed in Claim 1, characterized in that the bond pads of the third portion and the corresponding contact pads for external coupling are mutually interconnected through:

- interconnects defined in the conductive layer at the first side of the carrier substrate, and
- vertical interconnects through the carrier substrate which on perpendicular projection on the conductive layer at the second side have a substantial overlap with the contact pads for signal transmission.

6. An electronic device as claimed in Claim 5, characterized in that

- a ground plane is defined in the conductive layer at the second side of the carrier substrate,
- the mutual distance between the interconnects and the dielectric thickness of the carrier substrate are chosen such that the interconnects have transmission line characteristics.

7. An electronic device as claimed in Claim 1 or 6, further comprising a mechanical stiffner layer at the first side of the carrier substrate.

8. An electronic device as claimed in Claim 1, further comprising spacer layer at the first side of the carrier substrate, which spacer layer is covered by a heat dissipation layer, which heat dissipation layer is in thermal contact with the semiconductor device at a face thereof opposite to the face comprising the bond pads.

9. An electronic device as claimed in Claim 8, wherein the heat dissipation layer is connected thermally to a heat sink at the carrier substrate.

10. An electronic device as claimed in Claim 1, further comprising a second semiconductor device that is provided with a direct path for ground and voltage supply connection from its bond pads to the second side of the carrier substrate, at which second side contact pads for ground and voltage supply connection are present.

11. A carrier substrate comprising a layer of dielectric material and having a first side and an opposed second side, with at each side an electrically conductive layer, at which first side bond pads for coupling to bond pads of a semiconductor device, and at which second side contact pads for external coupling are provided, the contact pads and the bond pads being electrically interconnected according to a desired pattern, the contacts pad being subdivided in a first portion for voltage supply connection, a second portion for ground connection and a third portion for signal transmission, the first and second portions of the bond pads are present laterally in an inner area and the third portion is present in an outer area laterally around the inner area,

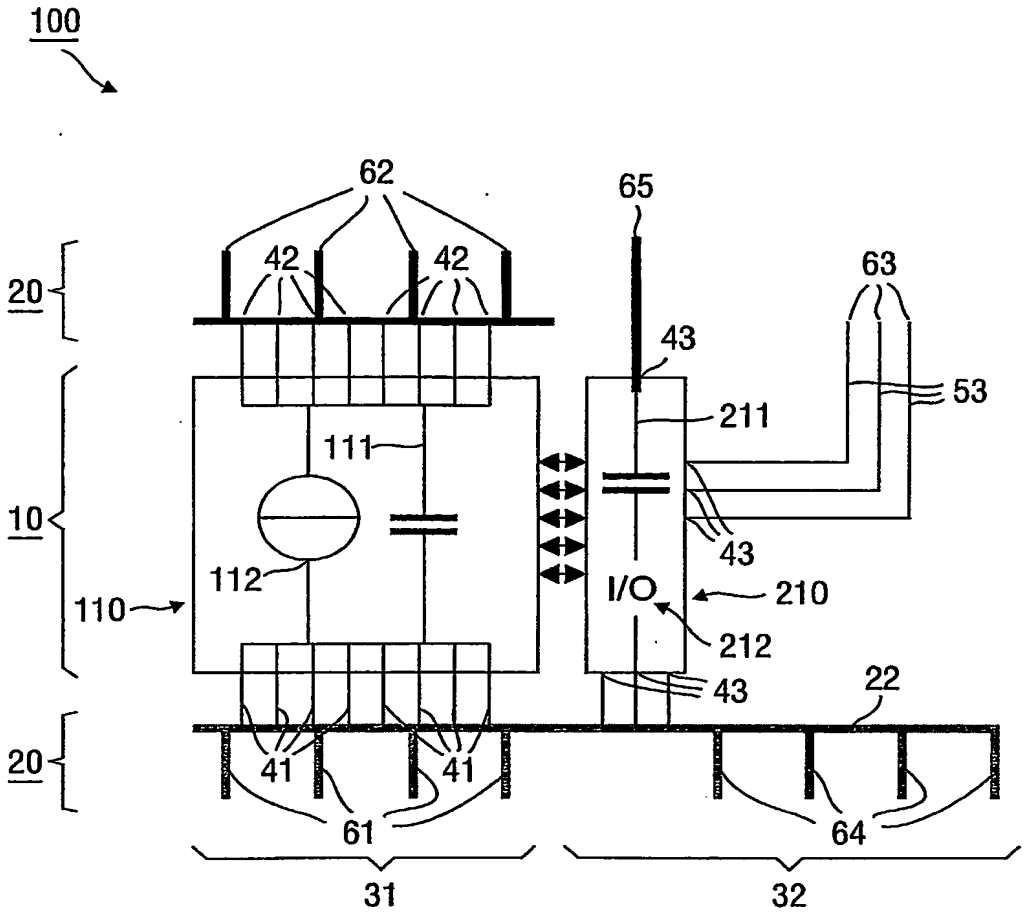
wherein

- the first and second portions of the bond pads make up an array jointly, which joint array extends to the contact pads at the second side of the carrier substrate, so as to form a direct path, and
- the pads for ground connection and for supply connection are arranged in the array such that each of the pads for supply connection has pads for ground connections as its closest neighbour pads.

ABSTRACT:

The electronic device comprises a semiconductor device (10), particularly an integrated circuit, and a carrier substrate (20) with conductive layers at the first side (21) and the second side (22), and voltage supply (62) and ground connections (61) mutually arranged according to a chessboard pattern. These connections (61,62) lead in a direct path through vertical interconnects and bumps (41,42) to bond pads at the integrated circuit, which bond pads are arranged in a corresponding chessboard pattern. Therewith, an array of direct paths is provided, wherein the voltage supply connections (62) form as much as possible the coaxial center conductors of a coaxial structure.

Fig. 4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42
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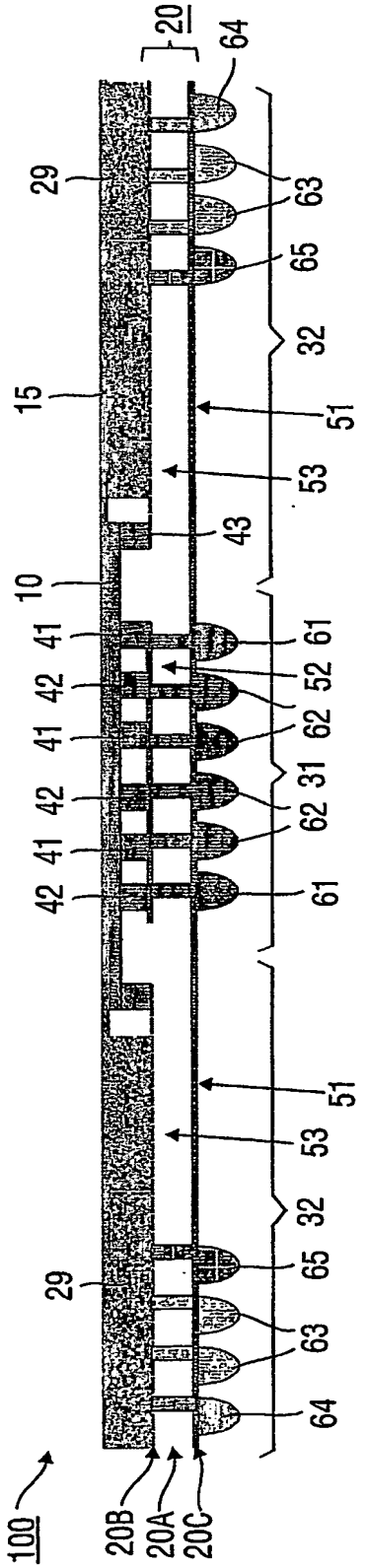
32

FIG.1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20A
20C

FIG.2

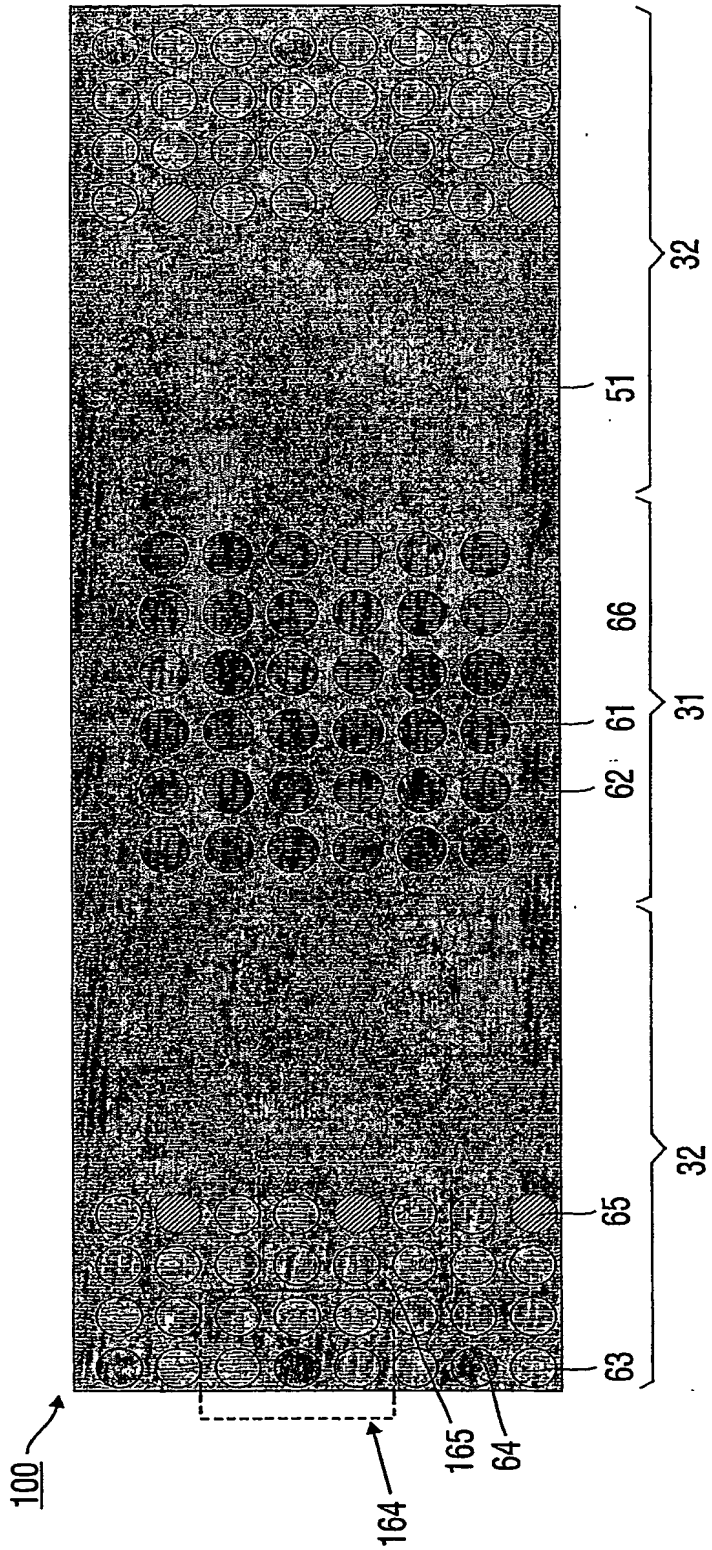

FIG.3

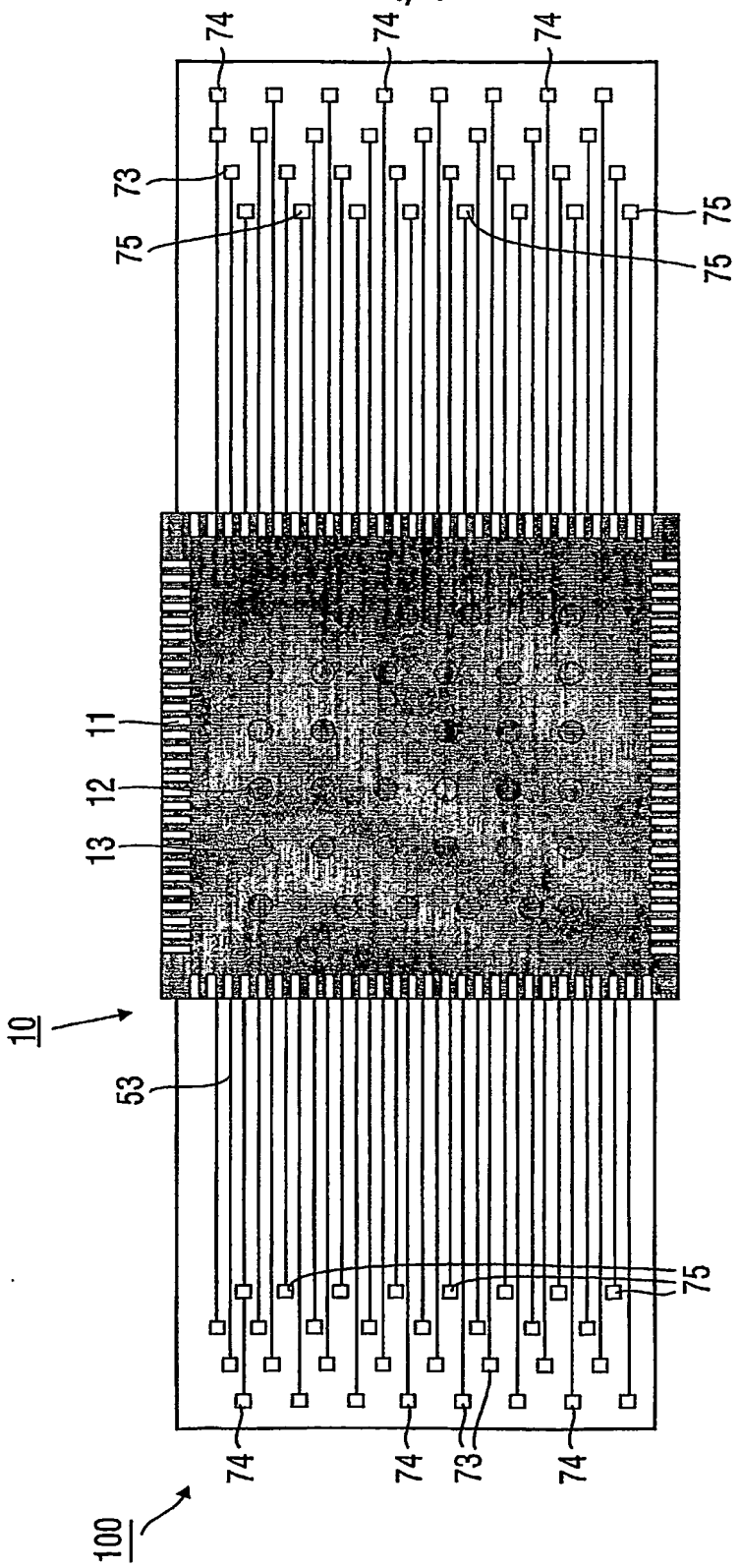

FIG.4